WE CLAIM:

1. An automatic test equipment (ATE) bidirectional drive channel for transmitting test signals to a device under test (DUT) and receiving signals from the DUT, comprising:

an input/output line for connection to a DUT,

a driver circuit connected to apply test signals to said input/output line for application to a DUT,

a receiver circuit connected to said input/output line to receive signals produced by a DUT, said receiver circuit having an associated capacitance, and

a first passive matching network connected to said line to at least partially compensate for said receiver circuit capacitance.

2. The ATE drive channel of claim 1, said first passive matching circuit comprising a T-coil circuit.

3. The ATE drive channel of claim 2, wherein said driver and receiver circuits are implemented on a common layer of an integrated circuit (IC), and said T-coil circuit includes inductors that are implemented in a separate layer of said IC that is spaced from said common layer by at least a dielectric layer.

4. The ATE drive channel of claim 3, further comprising a flip-chip bump having an associated redistribution layer at the same level as said T-coil inductors.

5. The ATE drive channel of claim 1, said driver circuit comprising the combination of a current-mode driver having an associated capacitance and a voltage-mode driver, said receiver circuit comprising a compara-

tor circuit for comparing a signal received from a DUT to a reference, further comprising a second passive matching network connected in series with said first passive matching network to at least partially compensate for said current-mode driver capacitance.

6. The ATE drive channel of claim 5, said first and second passive matching circuits comprising respective T-coil circuits.

7. An automatic test equipment (ATE) receive channel for receiving signals from a device under test (DUT), comprising:

an output line for connection to a DUT,

at least one receiver circuit connected to said output line to receive signals produced by a DUT, said receiver circuit having an associated capacitance, and

a passive matching network connected to said line to at least partially compensate for said receiver capacitance.

8. The ATE receive channel of claim 7, said passive matching circuit comprising a T-coil circuit.

9. The ATE receive channel of claim 8, wherein said receiver circuit is implemented on one layer of an integrated circuit (IC), and said T-coil circuit includes inductors that are implemented in a separate layer of said IC that is spaced from said first layer by at least a dielectric layer.

10. The ATE receive channel of claim 9, further comprising a flip-chip bump having an associated redis-

tribution layer at the same level as said T-coil inductors.

11. A capacitance-compensated circuit package, comprising:

an integrated circuit (IC) structure that includes a circuit layer with an associated capacitance,

a dielectric layer over said circuit layer,

a T-coil circuit over said dielectric layer, and

electrically conductive connectors extending through said dielectric layer to connect said T-coil circuit to said circuit layer so that said T-coil circuit at least partially compensates said capacitance.

12. The circuit package of claim 11, further comprising a metallization network overlying said circuit layer and making electrical contact therewith through a second dielectric layer, said T-coil circuit connected to said circuit layer via said metallization network.

13. The circuit package of claim 12, further comprising a flip-chip bump connected to said circuit layer and having an associated redistribution layer at the same level as said T-coil inductors.

14. A method of compensating for capacitance in an integrated circuit (IC), comprising:

fabricating an IC package having an electrical circuit with an unwanted capacitance,

providing a first dielectric layer over said IC package,

forming a T-coil circuit with inductors that are on said first dielectric layer, and

connecting said T-coil circuit through said first dielectric layer to said electrical circuit to at least partially compensate said capacitance.

15. The method of claim 14, wherein said T-coil circuit is formed and connected to said electrical circuit by forming openings through said dielectric layer, depositing a conductive material through said openings, and establishing said T-coil circuit on said dielectric layer in contact with said conductive material.

16. The method of claim 15, wherein said IC package is fabricated with a second dielectric layer over said electrical circuit, and a metallization network on said second dielectric layer and extending through said second dielectric layer to contact said electrical circuit, and wherein said T-coil circuit is connected to said electrical circuit via said metallization network.

17. The method of claim 16, wherein said IC package is fabricated with a passivation layer over said second dielectric layer and metallization network, openings are formed through said passivation layer in registration with said first dielectric layer openings, and said conductive material is deposited through said openings in both the first dielectric and passivation layers.

18. The method of claim 14, said electrical circuit comprising a bi-directional automatic test equipment (ATE) drive channel having a driver circuit connected to generate test signals for a device under test (DUT) and a receiver circuit for receiving signals generated by a DUT, said T-coil circuit comprising a first T-coil cir-

cuit that at least partially compensates for capacitance associated with said receiver circuit.

19. The method of claim 18, said driver circuit comprising the combination of a current mode driver having an associated capacitance and a voltage-mode driver, said receiver circuit comprising a comparator circuit for comparing a signal received from a DUT to a reference, further comprising forming a second T-coil circuit on said dielectric layer and connecting said second T-coil circuit through said dielectric layer to at least partially compensate the capacitance associated with said current-mode driver.

20. A capacitance-compensated circuit package, comprising:

a substrate,

an electrical circuit layer on said substrate, said electrical circuit layer having an associated capacitance,

a first dielectric layer over said circuit layer,

a second dielectric layer over said first dielectric layer,

a T-coil circuit having inductors in said second dielectric layer,

a flip-chip bump over said second dielectric layer, and

a redistribution layer for said flip-chip bump in said second dielectric layer,

said T-coil circuit and redistribution layer connected to respective portions of said electrical circuit layer through said first dielectric layer, with said T-coil circuit at least partially compensating said ca-

pacitance, and said flip-chip bump connected to said redistribution layer.

21. The circuit package of claim 20, further comprising a metallization network overlying said circuit layer end making electrical contact therewith through a further dielectric layer, said T-coil circuit and redistribution layer connected to said circuit layer via said metallization network.